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1	Sub	62. A data processor performing data processing
<u>2</u>	Ai7	based on an 8-bit instruction, the instruction independently
<u>3</u>	11	designating:
<u>4</u>	,	one of a plurality of operations including transfer
<u>5</u>		and calculation;
<u>6</u>		one of a plurality of registers as a source operand,
<u>7</u>		and /
<u>8</u>		one of the plurality of registers as a destination
9		operand;
<u>10</u>		wherein the plurality of registers includes at least
<u>11</u>		one register storing an address exceeding 16 bits.
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1 1 1 2		63. A data processor performing data processing
<u>2</u>		based on an 8-bit instruction, the instruction independently
		designating:
3 5 4		one of a plurality of operations including transfer
<u>5</u>		and calculation;
<u>6</u>		one of a plurality of registers as a source operand,
<u>6</u> <u>7</u>		and /
<u>8</u> <u>8</u>		one of the plurality of registers as a destination
<u> </u>		operand;
<u>10</u>		wherein at least one instruction is further followed
<u>11</u>		by a numeric gode of more than 16 bits.
<u>1</u>		A data processor performing data processing
<u>2</u>		based on/an 8-bit instruction, the instruction independently
<u>3</u>		designating:
<u>4</u>		one of a plurality of operations including transfer
<u>5</u>		and calculation;
<u>6</u>		one of a plurality of registers as a source operand,
<u> </u>		and
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<u>8</u>	one of the plurality of registers as a destination
<u>9</u>	operand;
<u>10</u>	wherein a first register and a second register are
<u>11</u>	included in the plurality of regsiters, and
<u>12</u>	a judgement of which one of sign-extending and
<u>13</u>	zero-extending is to be performed on operand data is made
<u>14</u>	depending on which of the first register and the second
<u>15</u>	register is designated as the destination operand in the
<u>16</u>	instruction.
<u>1</u>	65. A data processor performing data processing
<u> </u>	based on an 8-bit instruction the instruction independently
4 3 4 5 5 1 5 1 5 1 5 1 5 1 5 1 5 1 5 1 5 1	designating:
th <u>4</u>	one of a plurality of operations including transfer
<u> </u>	and calculation;
<u>6</u>	one of a plurality of registers as a source operand,
<u> </u>	and /
### 8 9 9 11 10 11 11 11 11 11 11 11 11 11 11 11	one of the plurality of registers as a destination
<u> </u>	operand;
<u> 10</u>	wherein an address register and a data register are
1 <u>11</u>	included in the plurality of registers, and
<u>12</u>	an address stored in the address register is longer
<u>13</u>	than data stored in the data register.
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